Listing of Claims

Claim 1 (currently amended). A tracing method, comprising:

detecting ~~an operating state~~ a processor mode of a processor and an application space identity (ASID) value defining an identity of a task being run on said processor~~, said processor having a plurality of operating states that include a plurality of processor modes~~;

receiving control signals defining ASID values and processor modes for which tracing is triggered; and

effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values ~~operating state of said processor and upon a control input for said current operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state~~.

Claim 2 (canceled).

Claim 3 (previously presented). The method of claim 1, wherein an indication of said control input for said current operating state is obtained via a software-settable trace control register.

Claim 4 (canceled)

Claim 5 (previously presented). The method of claim 1, wherein said processor modes comprise at least one of a kernel mode, a supervisor mode, a user mode, and a debug mode.

Claim 6 (previously presented). The method of claim 5, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on a MIPS32™ or MIPS64™ architecture specification.

Claim 7 (canceled).

Claim 8 (canceled).

Claim 9 (canceled).

Claim 10 (currently amended). The method of claim 1, wherein said ~~operating states include an identity of a process running on said processor and~~ tracing is triggered based on G, ASID, U, K, S, DM, and X controls, wherein said G if asserted, implies that all processes are to be traced, whereas if G is not asserted, trace data is processed for a current ASID value, ~~ASID is an application space identity,~~ U, if asserted, enables tracing in user mode, K, if asserted enables tracing in kernel mode, S, if asserted, enables tracing in supervisor mode, DM, if asserted, enable tracing in a debug mode, and X, if asserted, enables tracing for exception and error level conditions, said controls enabling tracing when:

((G is asserted OR (ASID equals a current process application space identity value)) AND

((U is asserted AND said processor is in user mode) OR

(K is asserted AND said processor is in kernel mode) OR

(S is asserted AND said processor is in supervisor mode) OR

(DM is asserted AND said processor is in debug mode) OR

(X is asserted AND (an exception level bit is asserted OR an error level bit is asserted)))).

Claim 11 (currently amended). A tracing system, comprising:

a processor core for executing instructions; and

trace generation logic that detects a processor mode ~~an operating state~~ of said processor core ~~said processor core having a plurality of operating states that include a plurality of processor modes~~ and an application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values ~~current operating state of said processor and upon a control input for said operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state~~.

Claim 12 (canceled).

Claim 13 (previously presented). The tracing system of claim 11, wherein said control input is identified via a software-settable control register.

Claim 14 (canceled).

Claim 15 (previously presented). The tracing system of claim 11, wherein said processor modes include at least one of a kernel mode, a supervisor mode, a user mode, and a debug mode.

Claim 16 (previously presented). The tracing system of claim 15, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on a MIPS32™ or MIPS64™ architecture specification.

Claim 17 (previously presented). The tracing system of claim 11, wherein said operating state includes an identity of a process being run on said processor and said predefined trace control is based on a current processor mode and said identity of a process.

Claim 18 (canceled).

Claim 19 (canceled).

Claim 20 (currently amended). The tracing system of claim 11, wherein said trace generation logic triggers tracing based on G, ASID, U, K, S, DM, and X controls, wherein said G if asserted, implies that all processes are to be traced, whereas if G is not asserted, trace data is processed for a current ASID value, ~~ASID is an application space identity,~~ U, if asserted, enables tracing in user mode, K, if asserted enables tracing in kernel mode, S, if asserted enables tracing in supervisor mode, DM, if asserted, enable tracing in a debug mode, and X, if asserted, enables tracing for exception and error level conditions, said controls enabling tracing when:

((G is asserted OR (ASID equals a current process application space identity value)) AND

((U is asserted AND said processor is in user mode) OR

(K is asserted AND said processor is in kernel mode) OR

(S is asserted AND said processor is in supervisor mode) OR

(DM is asserted AND said processor is in debug mode) OR

(X is asserted AND (an exception level bit is asserted OR an error level bit is asserted)))).

Claim 21 (currently amended). A computer program product comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a ttrace generation logic that detects a processor mode ~~an operating state~~ of said processor core ~~said processor core having a plurality of operating states that include a plurality of processor modes~~ and an

application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values ~~current operating state of said processor and upon a control input for said operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state~~; and

a computer-usable medium configured to store the computer-readable program codes.

Claim 22 (currently amended). A method for enabling a computer to generate a tracing system, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe atrace generation logic that detects a processor mode ~~an operating state~~ of said processor-core ~~said processor core having a plurality of operating states that include a plurality of processor modes~~ and an application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical

comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values ~~current operating state of said processor and upon a control input for said operating state, each particular operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state~~.

Claim 23 (original). The method of claim 22, wherein computer-readable program code is transmitted to said computer over the Internet.

Claim 24 (currently amended). A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions; and

computer-readable program code for causing a computer to describe a trace generation logic that detects a processor mode ~~an operating state~~ of said processor ~~core said processor core having a plurality of operating states that include a plurality of processor modes~~ and an application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values ~~current operating state of said processor and upon a control input for said operating state, each particular~~

~~operating state having a corresponding control input that determines whether tracing is enabled in said particular operating state, whereby tracing control is automatically adjusted when said processor transitions from one operating state to another operating state~~.